REMARKS

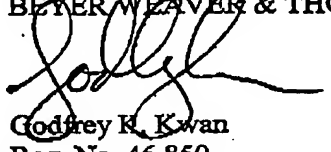
Claims 1-35 are pending. Claims 1-35 were rejected. Claims 1-32 were rejected under 35 U.S.C. 102(e) as being anticipated by Edirisooriya (2003/0195939A1), hereinafter Edi. Claims 33-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Edi.

Edi describes a multiprocessor system that "includes a plurality of processors 12 and 14 that are communicatively coupled via an interconnection network 16. The processors 12 and 14 are implemented using any desired processing unit ... The interconnection network 16 is implemented using any suitable shared bus or other communication network or interface that permits multiple processors to communicate with each other and, if desired, with other system agents such as, for example, memory controllers ... Additionally, the processors 12 and 14 respectively include caches 22 and 24, cache controllers 26 and 28 and request queues 30 and 32." (Paragraphs 12-14) Edi also describes use of the MSI, MESI and MOESI protocols "to eliminate unnecessary data transfers between processors." (Paragraph 33) Edi does not mention multiple processor clusters and only describes multiple processors connected over an interconnection network such as a shared bus.

By contrast, the independent claims 1, 16, 26 and 33 all recite a "home cluster" including a "plurality of processing nodes" and a "remote cluster" including a "plurality of processing nodes." A home cluster and a remote cluster are described throughout the present application and examples are depicted throughout in the Figures, e.g. Figures 1A, 1B, 2, 11, and 12 and associated description. Edi does not teach or suggest any home cluster or remote cluster. Furthermore, Edi does not teach or suggest any home cluster including a plurality of processing nodes or any remote cluster including a plurality of processing nodes. The Examiner argues that a remote cluster is "other processing nodes 14" shown in Figure 1 of Edi. The Applicants respectfully disagree. Edi merely depicts a conventional architecture in Figure 1 and associated description with a processor 12 connected to a processor 14 over a shared bus 16. No clusters are shown. No clusters of processing nodes are shown. The flows charts in Figures 2 and 3 and the associated description merely depict interactions between multiple processors connected over a bus 16. Figures 4a-4d and associated description also similarly only show "various states through which the multiprocessor system 10 shown in FIG. 1 progresses." No clusters are depicted, taught, or even suggested. Consequently, the rejections to independent claims 1, 16, 26, and 33 are believed overcome.

In light of the above remarks relating to independent claims the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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